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Heteroepitaxial Growth of Gold Nanostructures on Silicon by Galvanic Displacement

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ABSTRACT This work focuses on the synthesis and interfacial characterization of gold nanostructures on silicon surfaces, including Si(111), Si(100), and Si nanowires. The synthetic approach uses galvanic displacement, a type of electroless deposition that takes place in an efficient manner under aqueous, room-temperature conditions. The case of gold-on-silicon has been widely studied and used for several applications and yet, a number of important, fundamental questions remain as to the nature of the interface. Some studies are suggestive of heteroepitaxial growth of gold on the silicon surface, whereas others point to the existence of a silicon—gold intermetallic sandwiched between the metallic gold and the underlying silicon substrate. Through detailed high resolution transmission electron microscopy (TEM), combined with selected area electron diffraction (SAED) and nanobeam diffraction (NBD), heteroepitaxial gold that is grown by galvanic displacement is confirmed on both Si(100) and Si(111), as well as silicon nanowires. The coincident site lattice (CSL) of gold-on-silicon results in a very small 0.2% lattice mismatch due to the coincidence of four gold lattices to three of silicon. The presence of gold—silicon intermetallics is suggested by the appearance of additional spots in the electron diffraction data. The gold—silicon interfaces appear heterogeneous with distinct areas of heteroepitaxial gold on silicon, and others, less well-defined, where intermetallics may reside. The high resolution cross-sectional TEM images reveal a roughened silicon interface under these aqueous galvanic displacement conditions, which most likely promotes nucleation of metallic gold islands that merge over time: a Volmer—Weber growth mechanism in the initial stages.

KEYWORDS: gold nanoparticles · silicon surfaces · silicon nanowires · electron microscopy · galvanic displacement · heteroepitaxy · intermetallics

Interfacing metals with semiconductor surfaces at the nanometer scale has received much attention[1] as a result of the critical importance of these interfaces for applications such as integrated circuits,[2−4] optoelectronics,[5,6] and others.[7,8] An efficient and versatile approach for the synthesis of metallic nanostructures on semiconductors is galvanic displacement, a spontaneous electrochemical reaction that is a member of the electroless deposition family.[9−51] In this class of reactions, sufficiently oxidizing metal ions, with a redox potential more positive than that of substrate, are reduced by electrons derived from the bonding electrons of the substrate lattice valence band; the reaction is accompanied by substrate dissolution and occurs in the absence of an external source of electric current or chemical reducing agents.[42] The result is metallic nanoparticles and films interfaced directly with the substrate surface.[13,42] Because the reaction is carried out at room temperature with the simplest of chemical apparatus (water, metal ion, substrate in a beaker), it is straightforward to carry out and is less expensive and faster than commonly used metal evaporation[52,53] and sputtering techniques.[5,54]

Galvanic displacement has seen application in a number of different areas, particularly those related to the construction of nanoscale metallic and semiconductor architectures. For instance, Carraro and co-workers used galvanic displacement to produce gold nanoparticle catalyst arrays in silicon trenches for the synthesis of horizontally suspended silicon nanowires (NWs).[11] Gösele and co-workers demonstrated that gold nanoparticles on silicon surfaces, prepared *via* galvanic displacement, resulted in the growth of a high quantity of epitaxial Si nanowires with neat and sharp crystallographic interfaces, whereas evaporated gold films led to low amounts of epitaxial nanowires, with defects at the silicon nanowire—bulk silicon interface.[55,56] The group of Kamins and co-workers from Hewlett-Packard (HP) demonstrated galvanic displacement directly on silicon nanowires to produce gold nanoparticle-decorated silicon nanostructures.[49] Galvanic displacement has also been found to be amenable to nanoscale patterning *via* self-assembled block copolymer templates, reverse micelle deposition on surfaces, and dip-pen nanolithography (DPN) to produce, in a controlled manner, metallic nanostructures on a variety of different semiconductor interfaces.[11,17,32,57] In a completely unrelated application, galvanic displacement

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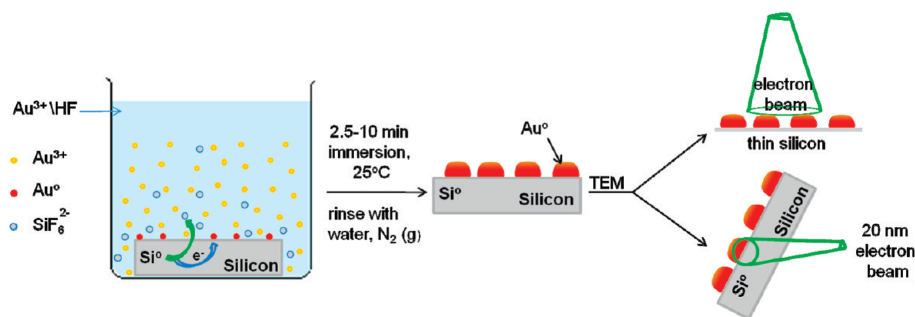


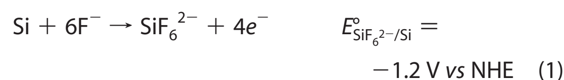
Figure 1. A silicon substrate is immersed in a mixture of a gold salt, [$KAuCl_4$ (aq) and HF (aq)] at room temperature. Galvanic displacement occurs when the semiconductor surface acts as the electron source for the reduction of the metal salt. HF (aq) is required to ensure the formation of soluble SiF_6^{2-}(aq) and related species from the resulting oxidized silicon to allow for continued electron transfer. Transmission electron microscope (TEM) investigations were then carried out on backside thinned planar and cross-sectioned samples.

of silver nanoparticles on silicon can be used to etch silicon nanowire arrays in a wet chemical fashion.[58]

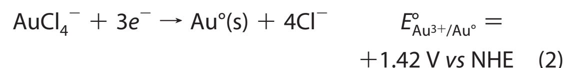
Although gold-on-silicon nanostructures, prepared by galvanic displacement, have been used in the fabrication of many device architectures, the Au−Si interface is not well understood, and is the source of much interest. A detailed understanding of the nature and the structure of the gold−silicon interface as prepared by galvanic displacement, and the subsequent growth mode of the gold nanostructures merits detailed consideration not only from a technological perspective, but also to elucidate fundamentals in interfacial nanoscience.[11,32,44,45] In terms of galvanic displacement of metals on semiconductors, a number of basic questions remain that do not yet allow for a convergent set of conclusions to be made as to the nature of these interfaces. For instance in the case of gold on silicon, XPS depth profiling clearly indicates evidence for the existence of undefined interfacial gold−silicon intermetallics,[10] whereas surface X-ray diffraction studies point to heteroepitaxial growth of gold on silicon;[46] the relationship or connection between the presence of intermetallics and heteroepitaxy is difficult to envisage. In addition to questions regarding the growth mechanism of metallic nanoparticles on semiconductors *via* galvanic displacement, both Volmer−Weber[37,38,46,47] and Stranski−Krastanov modes[48] of growth have been suggested. To attempt to answer some of these questions, we harnessed the precision of transmission electron microscopy (TEM) nanobeam diffraction analyses to characterize, in detail, the nature of gold−silicon interfaces formed *via* galvanic displacement on flat single crystal Si(111) and Si(100) surfaces, and silicon nanowires.

RESULTS AND DISCUSSION

The synthesis of gold nanostructures on silicon surfaces was carried out through immersion of a semiconductor wafer in a solution of metal ions with a sufficiently high oxidation potential; this reaction, galvanic displacement, occurs spontaneously as outlined in Figure 1. The reaction is essentially a corrosion reaction in conjunction with metal deposition—the semiconductor acts as a source of electrons that reduce the metal ions in solution to M(0) on the surface, while surface atoms are oxidized and solubilized either locally and/or distally, from an exposed surface.[13,18,42] In the case of silicon, hydrofluoric acid is required to ensure continuous metallic growth since the spontaneously formed silicon oxide product is a dielectric, and would prevent further metal ion reduction. In the presence of HF (aq), the silicon oxide layer is dissolved *in situ* to form soluble SiF_6^{2-} (aq) species according to eq 1:[28]



$$Si + 6F^- \rightarrow SiF_6^{2-} + 4e^- \qquad E^\circ_{SiF_6^{2-}/Si} = -1.2\ \mathrm{V}\ vs\ \mathrm{NHE} \quad (1)$$



$$AuCl_4^- + 3e^- \rightarrow Au^\circ(s) + 4Cl^- \qquad E^\circ_{Au^{3+}/Au^\circ} = +1.42\ \mathrm{V}\ vs\ \mathrm{NHE} \quad (2)$$

Figure 2 shows the formation of nanostructured gold films on single crystal shards of Si(111) and Si(100), and silicon nanowires, by immersion in dilute $KAuCl_4$ (aq) and HF (aq) for short periods of time (seconds to minutes). Plan view (top view) SEM images reveal more continuous growth of gold on Si(111) as opposed to Si(100), but cross-section SEM images show no appreciable difference in the thickness of the gold layer, ~10 nm in each case. On silicon nanowires, gold nanoparticles of different sizes (20−30 nm) are observed. Longer immersion times results in greater quantities of metallic deposition on all of the silicon surfaces studied, as expected (Supporting Information).[14,49]

Heteroepitaxial Growth of Gold Nanoparticles on Silicon Surfaces. To characterize the structure and morphology of the gold nanoparticle layer topping the silicon, the substrates were characterized by high resolution transmission electron microscopy (HRTEM) and electron diffraction (beam size *ca.* 20−100 nm). To carry out TEM, the flat hydrogen-terminated silicon surfaces (500 μm-thick wafer shards) were immersed in a 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq) solution for 2.5 min, and then the backside of the silicon shard was mechanically polished until the silicon was thinned to less than a micrometer to permit TEM imaging. Shorter immersion times were used to ensure a thin gold layer appropriate for plan view TEM (2.5 min *versus* 7.5 min). Figure 3a shows, for example, the plan view bright field (BF) TEM image for a gold film on a Si(111) substrate; the dark areas are the gold deposits, whereas the lighter areas correspond to the silicon substrate. To investigate the orientation of the gold layer with respect to the underlying silicon

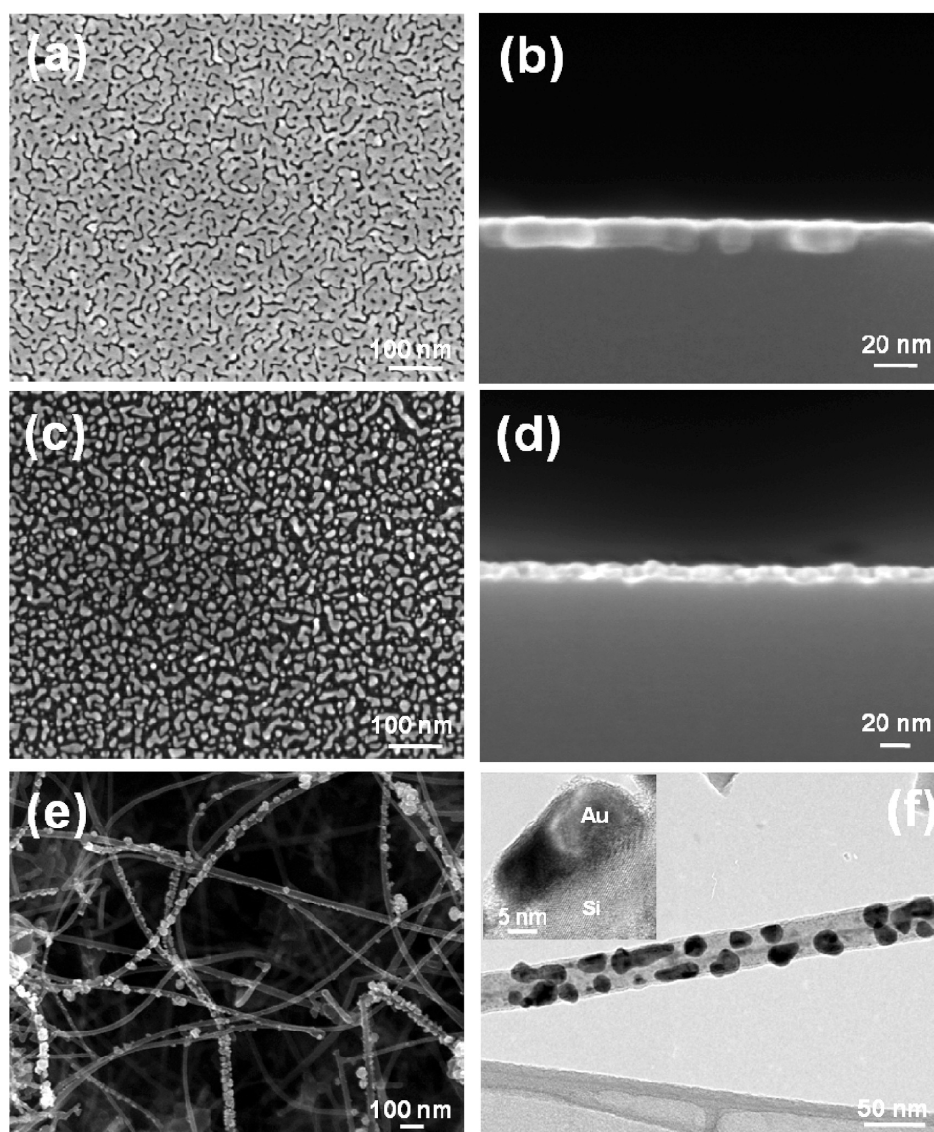


Figure 2. Scanning electron micrographs and transmission electron micrographs for gold galvanically displaced on silicon surfaces. (a and b) Plan view and cross-section SEM images of Au films on Si(111) formed from 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 7.5 min. (c and d) Plan view and cross-section SEM images of Au films on Si(100), formed from 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 7.5 min. (e) SEM image of silicon nanowires functionalized with gold nanoparticles. Conditions: 1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 30 s. (f) TEM image for gold nanoparticles on a silicon nanowire following removal of the Si nanowires in panel e from their substrate *via* sonication in 100% ethanol, followed by spotting the supernatant layer on a lacy-carbon grid. The inset shows HRTEM image of a Si nanowire with a single gold nanoparticle.

planes, low and high resolution TEM images were taken along the $[\bar{1}12]$ zone axis of silicon (Figure 3b,c). The Moiré-fringes of the gold layer on $Si(1\bar{1}1)$ are visible. TEM images along the $[\bar{1}23]$ zone axis are similar and are shown in the Supporting Information. The fringe spacing *D*, measured from the marked area in Figure 3b, is 9.5 Å. To calculate the theoretical fringe spacing, *D*, the following equation is used:[59]

$$D = \frac{d_{Si\{111\}} d_{Au\{111\}}}{d_{Si\{111\}} - d_{Au\{111\}}} \quad (3)$$

where $d_{Si\{111\}}$ (3.134 Å) and $d_{Au\{111\}}$ (2.355 Å) are the interplanar spacings for the silicon {111} and gold {111} planes, respectively. On the basis of the lattice parameters of the gold and silicon {111} planes, *D* is calculated to be 9.47 Å, identical within experimental error to the observed value of 9.5 Å. Therefore, the Moiré-fringes are parallel to both the gold and silicon planes. Such alignment is suggestive of an epitaxial relationship in which a single crystalline layer of gold is oriented in a parallel manner on the single crystalline Si(111),[59−61] as has been suggested for galvanic displacement of gold on silicon-based surface X-ray diffraction spectroscopy results.[46]

To confirm the epitaxial relationship between gold and silicon, selected area electron diffraction (SAED, beam size ≈ 100 nm) was taken along the $[\bar{1}12]$ zone axis (Figure 3d). The silicon pattern consists of spots, due to its single crystal nature, arising from diffraction from the $(1\bar{1}1)$, (220), and $(13\bar{1})$ planes; gold shows dif-

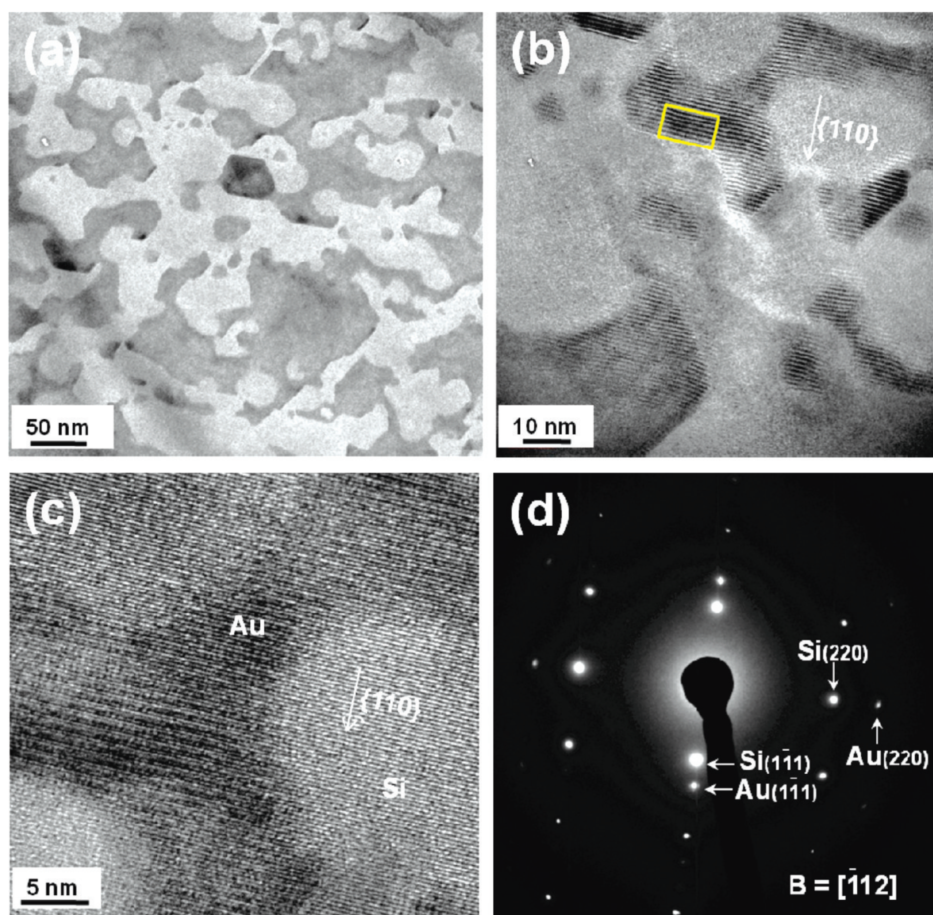


Figure 3. Transmission electron micrographs for a gold film on Si(111), formed by immersing the silicon substrate in 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 2.5 min. (a) Plan view bright field (BF) TEM image. (b and c) HRTEM images taken close to the [$\bar{1}$12] zone axis. (d) Selected area electron diffraction (SAED) pattern taken along the [$\bar{1}$12] zone axis. The yellow box in image b marks the area used to calculate the fringe spacing *D* in eq 3.

fraction from these same planes. Other features of note include the parallel feature of the {112} family of crystallographic planes, of both the silicon substrate and the gold overlayer. The gold (1$\bar{1}$1) and (220) planes are parallel to the silicon (1$\bar{1}$1) and (220) planes, respectively: Au(1$\bar{1}$1)//Si(1$\bar{1}$1) and Au(110)//Si(110). Hence, the SAED pattern is strongly indicative of the Au(111)[$\bar{1}$12]// Si(111)[$\bar{1}$12] in-plane epitaxial relationship of the gold-on-silicon. Further investigation by XRD (Supporting Information) for thicker gold films on Si(111) immersed in 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 20 min showed gold peaks for only the (111) and (222) planes, indicating the single crystal nature of the gold overlayer and the preferential growth of the gold layer along the ⟨111⟩ growth direction; the gold layer grew along the same crystallographic direction as the underlying substrate.

The phenomenon of heteroepitaxial crystallization involves the epitaxial growth of a layer (an epilayer) with a chemical composition and, typically, structural parameters different from those of the substrate.[61] Lattice mismatch or misfit (the disregistry of the interfacial atomic arrangement of the substrate and the overgrown epilayer) is known to have a significant effect on epitaxy.[61] Au(111) and Si(111) with interplanar *d* spacings of 2.355 and 3.134 Å, respectively, have about a 25% lattice mismatch. By considering the coincident site lattice interface (CSL), however, in which three silicon lattices match with four gold lattices, $4xd_{Au(111)} = 9.420$ Å and $3xd_{(Si(111)} = 9.402$ Å, the lattice mismatch is only 0.2%. Such heteroepitaxy has previously been observed for evaporated gold on silicon following annealing at temperatures greater than 380 °C.[62] A CSL interface has been considered for the epitaxial growth of the electron-beam evaporated silver on Si(111) surfaces.[63]

To visualize the gold nanoparticle−silicon interfaces of Au/Si(111) and Au/Si(100) and confirm heteroepitaxy, cross-sectional high resolution TEM (HRTEM) investigations were carried out. Figure 4a shows cross-sectional HRTEM image for a gold nanocrystallite on Si(111) that reveals the coincidence of four gold lattice fringes with three silicon lattice fringes, as marked by the yellow and pink lines, respectively. In addition, the top epitaxial gold planes are clearly parallel to the direction of those of the underlying silicon substrate. Similar results were observed for Au/Si(100) as shown in Figure 4b. In the case of gold on Si(100) (Figure 4b), the gold−silicon interface displays a significant degree of heterogeneity—some areas have very clear coincident gold and silicon lattices, whereas others appear less ordered (Supporting Information). In the inset of Figure 4b, one ill-defined region is highlighted, the exact composition of which is as-of-yet unknown (*vide infra*).

Because prior literature contains much postulation regarding the existence of intermetallics (gold−silicides),[10,48] nanobeam diffraction with a 20 nm probe was utilized to glean further information about the interface between a single gold nanocrystallite and Si(111) and Si(100) surfaces, and Si nanowires. As shown in Figure 5, the heteroepitaxial gold−silicon relationship is visible from the nanobeam diffraction patterns of all the cross-sectional gold−silicon interfaces. Alignment of gold and silicon diffraction spots, marked by red and blue lines, respectively, indicates that the growth of the crystalline gold is in the direc-

tion of the underlying silicon planes; both materials diffract along the same zone axes. In the case of Si(111) and Si(100), diffraction patterns were taken along the [110] zone axis, and the [111] for the nanowires.

There are, however, diffraction spots that do not correspond to either gold or silicon planes, and have interplanar spacings unrelated to the marked gold or silicon planes (red/blue lines), as indicated in green in Figure 5a−d. It is possible that the extra spots on Si(100)/gold result from the presence of crystalline gold silicides (summarized in Table 1, Supporting Information). In Figure 5a for gold on Si(111), there are seven additional spots (in green), of which four can be indexed against the Au_2Si, Au_5Si, Au_7Si intermetallics. In Figure 5b for gold on Si(100), 11 additional spots are observed of which 9 can be indexed for intermetallics, and in Figure 5c, for a different region of gold on Si(100), 12 extra spots are observed of which 7 can be indexed for intermetallics. The spots in the Si(100) case correspond to the following intermetallics: Au_7Si, Au_4Si, Au_5Si, Au_5Si_2, Au_3Si_2, Au_3Si, and Au_2Si. Similarly, six extra spots are observed in the diffraction pattern for a gold nanoparticle on a silicon nanowire (Figure 5d), three of which can be indexed to the Au_2Si, Au_5Si, and Au_7Si intermetallics. Because the nanoprobe diffraction studies are certainly not comprehensive with respect to determination and characterization of gold silicides due to the very high complexity of the system, the characterization of these gold silicides cannot be considered complete. We surmise that the intermetallics reside in the ill-defined regions (*vide supra*, Figure 4b) since there is no evidence for involvement of foreign material in the Si/Au heteroepitaxial layers. The gold−silicon interfaces are therefore most likely composed of regions of heteroepitaxial gold-on-silicon, and separate domains containing an intermetallic sandwiched between the gold and silicon layers.

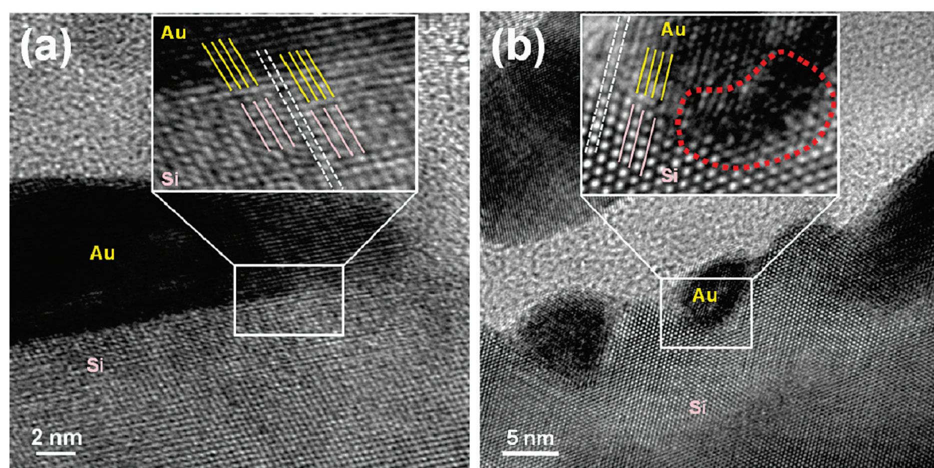


Figure 4. Cross-sectional HRTEM images for gold−silicon interfaces, formed by immersing the substrates in 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 7.5 min: (a) Si(111), (b) Si(100). The yellow and pink lines show the coincident site lattice interfaces for the gold and silicon planes, respectively. The area in panel b outlined in red highlights an ill-defined region of the gold−silicon interface. Both images were taken close to the [110] zone axis. The white lines show the alignment and the parallel nature of the gold epilayer to the underlying silicon substrates.

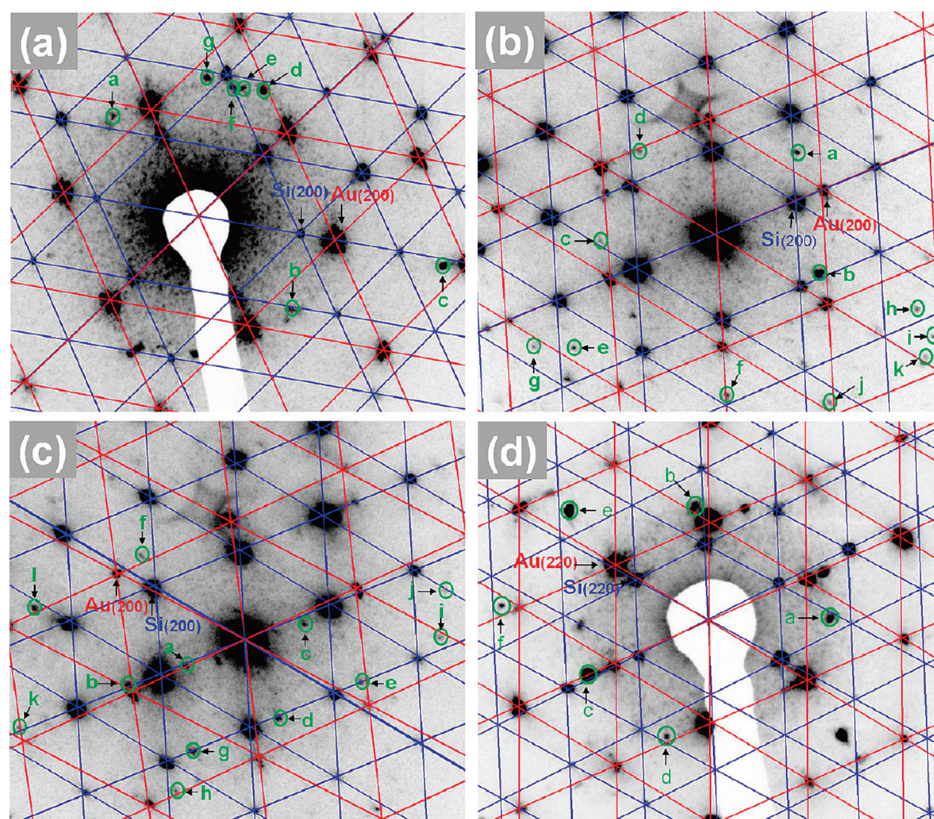


Figure 5. Nanobeam diffraction patterns (probe ≈ 20 nm) of gold-on-silicon samples. Blue and red lines correspond to silicon and gold planes, respectively. (a−c) Cross-sectioned gold-on-silicon wafers prepared through immersion of Si wafer shards in 0.1 mM $KAuCl_4$ (aq) + 1% HF (aq) for 7.5 min. Diffraction patterns were taken close to the [110] zone axis (a−c): (a) Si(111), (b,c) diffraction patterns for Si(100), taken at different locations. (d) Diffraction pattern, taken close to the [111] zone axis, from an interface between an individual gold nanoparticle and a silicon nanowire prepared using 1 mM $KAuCl_4$ (aq) and 1% HF (aq) for 30 s.

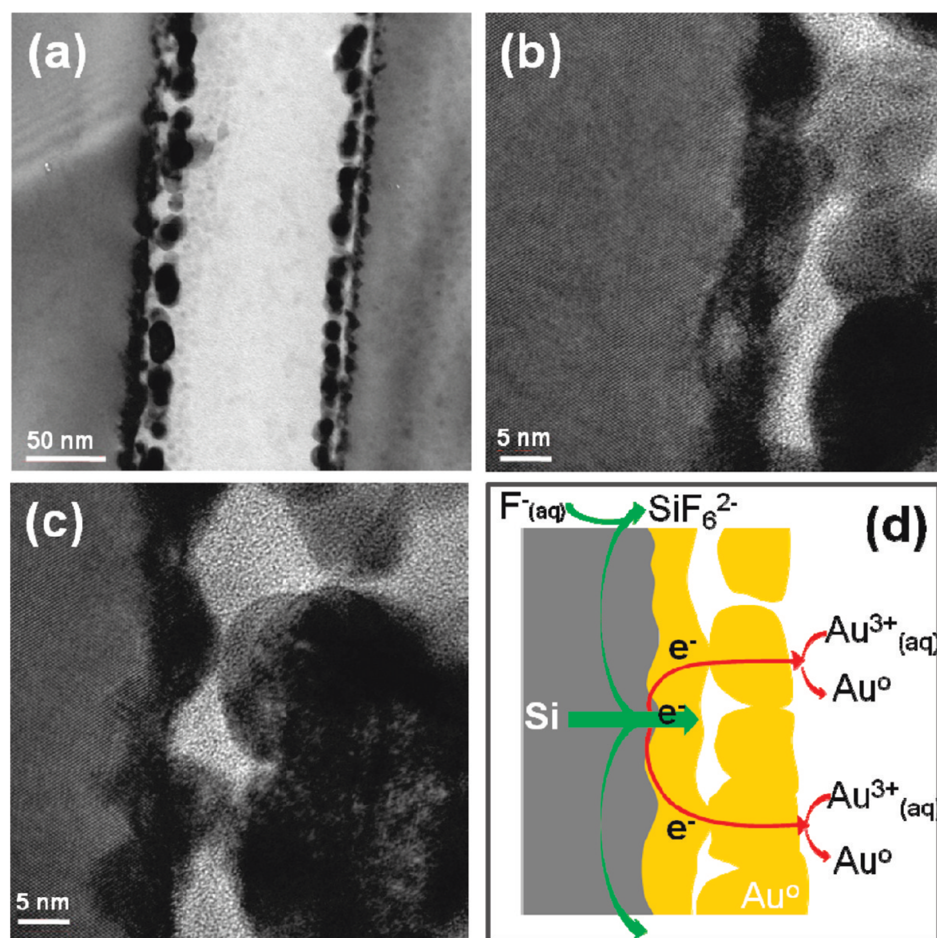


Figure 6. TEM images showing the growth mode of Au on Si(100). (a) Cross-section TEM image of gold-on-Si(100) grown by immersing the silicon substrate in 0.1 mM $KAuCl_4$ (aq) + 1% HF (aq) for 7.5 min. (b and c) Cross-section HRTEM images of the same sample shown in panel a. (d) Schematic diagram showing VW growth during the galvanic displacement process.

Figure 5b,c, as stated earlier, shows the nanobeam diffraction patterns for gold nanoparticle–Si(100) interfaces from different locations. Figure 5c shows an area in which the gold planes are tilted by about ~3.3° from the silicon planes. A 2.0° tilting was observed for Au planes on Si nanowires as well, Figure 5d. Crystallographic tilting of heteroepitaxial systems with their vicinal substrates is often observed;[64] for instance, tilting of heteroepitaxial gold and silver on silicon has been described previously,[46,52,65–67] and has been ascribed to misfit dislocation (disregistry of the epilayer and substrate planes),[64,66,68] or misfit between the height of a gold monolayer and a silicon step.[67] In the case of a silicon surface in an aqueous HF solution under galvanic displacement conditions, the surface will certainly not be flat, and thus surface roughness is most likely playing an important role in the observed epitaxial tilting, leading to defects and dislocations.

Epitaxy Growth Mode. For galvanic displacement of gold on silicon, two growth modes have been postulated to be in operation: the Stranski–Krastanov (SK) mode,[48] and Volmer–Weber (VW) growth.[37,38,46,47] The SK mode is common in lattice mismatched heteroepitaxial systems such as InAs on GaAs,[69,70] Ge on Si,[71] Ag on Si,[72] and Au on Si.[48,73,74] In the SK growth mode, a two-dimensional intermediate submonolayer forms and acts as a base for subsequent island growth.[61] Through their AFM studies of galvanic displacement of gold on silicon, Carraro and co-workers suggest surface morphology that is consistent with the SK mode of growth, in which the silicon surface is coated with a gold silicon silicide base monolayer, decorated with gold nanoparticles.[48] The SK mode was also postulated to be the growth mode for evaporated gold on Si(111) as judged *via* STM surface studies.[73,74] A three-dimensional (3D), island or Volmer–Weber (VW) growth mode has also been reported for the deposition of gold on silicon surfaces by galvanic displacement.[37,38,46,47] VW growth mode involves the nucleation of small clusters directly on the substrate surface followed by their subsequent growth into islands.[61] For galvanically displaced gold on silicon, AFM studies along with surface X-ray diffraction[46] and surface second harmonic generation[37,38,47] surface analyses reveal Au cluster formation which would be suggestive of a 3D or VW growth mechanism. To try to shed some light on the possible mechanism, detailed cross-sectional TEM imaging was employed, as shown in Figure 6 for Au/Si(100); similar results for Si(111) are observed (Supporting Information). Two silicon wafers were immersed for 7.5 min in a solution of 0.1 mM $KAuCl_4$ (aq) and 1% HF (aq), followed by gluing them together with a ~100 nm layer of M-Bond and then microtomed to form a sandwich less than one micrometer thick (details in the experimental section). As can be seen in Figure 6a–c, there is a ~5 nm thick layer of gold (gold lattice planes are visible), closely allied with the silicon substrate, capped by an overlayer of necked gold particles. The high resolution TEM images (Figure 6b,c) show that the ~5 nm gold layer is formed by the coalescence of gold nanoparticles that presumably grew from the initially formed nuclei on the rough (on the nanoscale) silicon surface. The rough nature of this interface results in scattered nucleation events,[21] followed by growth of metallic gold until the metal deposits make contact

with each other. The apparent overlayer of nanoparticle growth, above the initial gold−silicon contact, results from further deposition on the surface with longer immersion times in which the more closely silicon-bonded gold acts as the cathodic layer through which electron transport takes place. These electrons, produced from the corrosion of the exposed silicon surface (perhaps nearby or distal),[75−78] reduce gold ions in close vicinity in the solution to metallic gold, producing the necked particle overlayer. Figure 6d schematically illustrates a possible mechanism for the galvanic displacement process for gold on silicon, in which electrons from silicon dissolution promoted by fluoride ion lead to reduction of gold(III) complexes in the aqueous solution. The discrepancy between the observed results from different research groups most likely arises from the varying conditions used by each. If the conditions are such that deposition occurs on atomically flat hydride-terminated Si(111) planes, for instance, then an SK growth mode would be more likely. In our case, silicon surface roughening (on the nanoscale) is promoted by galvanic displacement,[57] and thus the VW growth appears to predominate, at least initially. The observed roughening of the interfaces during galvanic displacement is almost certainly the cause for VW island growth mode, and may also be the source of interfacial heterogeneity with respect to gold−silicon intermetallic formation, and heteroepitaxy.

CONCLUSIONS

Galvanic displacement is a useful approach for synthesizing metal-on-semiconductor interfaces for a range of applications. Through detailed TEM and nanobeam diffraction studies of galvanic gold deposition on silicon [Si(100), Si(111) and silicon nanowires], a better understanding of the interface between the silicon and the metallic gold was achieved. A heteroepitaxial relationship between the gold and silicon was confirmed, and was directly observed by high resolution TEM on both single crystal silicon shards and the nanowires, revealing a coincident site lattice of four gold to three silicon lattices (lattice mismatch of 0.2%). Nanobeam diffraction patterns taken from a 20 nm gold−silicon interfacial area reveal a host of spurious spots that are clearly not derived from known gold or silicon planes, but are suggestive of gold−silicon intermetallics. Finally, cross-section TEM images of microtomed samples reveal a rough silicon interface and nucleated island growth of gold that is suggestive of Volmer−Weber growth, under these conditions.

EXPERIMENTAL SECTION

Generalities. Unless otherwise noted, all experiments were performed under ambient laboratory conditions. Si(111) and Si(100) (p-type, B-doped, $\rho < 0.005\ \Omega \cdot cm$, 500 μm thickness) wafers were purchased from Silicon Quest International, Inc. $KAuCl_4 \cdot xH_2O$ was purchased from Strem Chemicals. Anchored silicon nanowires were grown by the vapor liquid solid technique on a p-type (B-doped) Si(100) substrate.[49,79]

Pretreatment of Silicon Substrates. All wafers were diced into 1 cm^2 pieces with a diamond scriber. Silicon shards were degreased in a methanol ultrasonic bath for 15 min and dried under a nitrogen stream. The wafers were then cleaned using the following standard RCA cleaning procedures.[16] The wafers were first immersed into a hot solution of H_2O:NH_4OH:H_2O_2 (5:1:1) for 15 min, and after rinsing with excess water, they were immersed into a hot solution of H_2O:HCl:H_2O_2 (6:1:1) for 15 min. The wafers were again rinsed with excess water and then dried under a stream of nitrogen. Following this cleaning procedure, the wafers were immersed into 1% HF (aq) for 7 min, to remove the native surface oxide film. The samples were then rinsed with water and dried under a nitrogen stream. In the case of silicon nanowires, the wafer was divided into smaller pieces. Each substrate was cleaned by immersion in a mixture of H_2SO_4:H_2O_2 (aq) (1:1) for 5 min.[49] The samples were then rinsed with distilled water and dried under nitrogen. To hydrogen passivate the silicon nanowires, the substrates were immersed in 1% HF (aq) for 3 min, then rinsed with water and dried under nitrogen.

Metal Deposition. The silicon wafer shard was immersed in the desired aqueous gold salt and hydrofluoric acid solution in a Teflon beaker. The gold salt/acid solutions were prepared by mixing 0.1 mL of 0.01 M $KAuCl_4 \cdot xH_2O$ and 9.9 mL of 1% HF (aq) for a given time. After metal deposition, the sample was thoroughly rinsed with water and dried under a nitrogen stream. In the case of silicon nanowires, a 10 μL drop of 1 mM $KAuCl_4$ (aq) and 1% HF (aq) was placed on the nanowire-coated substrate surface for 30 s, then rinsed with distilled water and dried under nitrogen.[49]

Surface Characterization. The gold nanostructures on the silicon surfaces were characterized by scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffraction (XRD). SEM (Hitachi S-4800 FE-SEM) of gold nanostructures was typically performed with an electron energy of 20 keV. TEM images and nanobeam electron diffraction patterns, using a probe of about 20 nm, were recorded on a 200 kV JEOL 2200FS TEM/STEM instrument, equipped with a high tilt cryo-polepiece. X-ray diffraction was performed on a Bruker D8 Discover instrument equipped with a sealed Cu tube. The peaks in the X-ray diffraction pattern were identified in terms of the Bragg angle, 2θ.

TEM Sample Preparation. For cross-sectional samples of Si(111) and Si(100), six gold−silicon samples were glued together using M-Bond. A 3 mm cylinder was then cut from the side of the six wafers using an ultrasonic cutter and this cylinder was then inserted into a copper cylinder with epoxy. The copper tube was cut by a diamond saw into small disks about 600 μm thick. Each disk was then polished on both sides to 100 μm thickness. A $\sim$1 μm thickness was achieved by dimpling from both sides. For plan view samples, the backside of the silicon shard was mechanically polished until the silicon was thinned to less than a micrometer. After achieving submicrometer thicknesses for both cross-section and plan view samples, ion milling was then used to create a small hole and clean the surface. Milling was done at low temperature (less than −100 °C with LN_2 cooling) at 6° milling angle, and with a voltage/current of 5 kV/3 mA at the beginning, and 0.5 kV/3 mA for final polishing. In the case of silicon nanowires, the substrate was immersed into a vial with 100% ethanol and ultrasonicated for 5 min. A drop of the supernatant layer was then spotted onto a lacy-carbon grid.

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Supporting Information Available: Additional SEM and TEM data for gold-functionalized interfaces. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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